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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO
10/738,408	12/16/2003	Kirk D. Prall	400.249US01	8316
27073 7:	590 09/15/2006		EXAMINER	
LEFFERT JAY & POLGLAZE, P.A.			DIAZ, JOSE R	
P.O. BOX 5810 MINNEAPOLI	009 IS, MN 55458-1009		ART UNIT PAPER NUMBER	
			2815	·
			DATE MAILED: 09/15/2006	

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
	10/738,408	PRALL ET AL.				
Office Action Summary	Examiner	Art Unit				
	José R. Díaz	2815				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status						
1) Responsive to communication(s) filed on 30 Au	igust 2006.					
,— .	action is non-final.					
·—						
closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims						
4)⊠ Claim(s) <u>1-6,9,11,12,14,15,17 and 19-22</u> is/are pending in the application.						
4a) Of the above claim(s) is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>1-6,9,11,12,14,15,17 and 19-22</u> is/are rejected.						
7) Claim(s) is/are objected to.						
8) Claim(s) are subject to restriction and/or election requirement.						
Application Papers						
9) The specification is objected to by the Examiner.						
10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).						
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority under 35 U.S.C. § 119						
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of:						
1. Certified copies of the priority documents have been received.						
2. Certified copies of the priority documents have been received in Application No						
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).						
* See the attached detailed Office action for a list of the certified copies not received.						
See the attached detailed Office action for a list of the certified copies not received.						
·						
Attachment(s)	A) [] [-1	(DTO 442)				
1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413) Paper No(s)/Mail Date						
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) 5) Notice of Informal Patent Application (PTO-152)						
Paper No(s)/Mail Date 6)						

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DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 30, 2006 has been entered.

Claim Rejections - 35 USC § 112

- 2. The following is a quotation of the second paragraph of 35 U.S.C. 112:
 - The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
- 3. Claims 1-6 and 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear to the examiner whether the claimed limitations "doping second regions" (as recited in the third step) and "a doped second region" (as recited in the fourth step) are related or refer to the same region.
- 4. Claims 2-6 and 9 are rejected due to their dependency on claim 1.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-6, 9, 11-12, 14-15, 17, 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (US Pat. No. 6,486,028 B1, previously cited by applicant).

Regarding claims 1, 11 and 20-22, Chang et al. teaches a method for making an array of memory cells configured to store at least one bit per one F² comprising:

incising (102) the substrate (100) to provide an array of edges having substantially vertical edge surfaces, pairs of the edge surfaces facing one another [see fig. 1];

doping (103) a first region (104) of a semiconductor substrate and second regions (108) between the pairs of edge surfaces [see fig. 2];

disposing respective structures each providing an electronic memory function on at least some respective ones of the edge surfaces, each structure having a gate insulator (110, 112, 114) formed on an edge surface and extending to a doped second region (108), and a control gate (116) formed on the gate insulator [see figs. 5-6]; and

establishing electrical contacts to the first and second regions [col. 1, lines 19-25].

In addition, Chang et al. teaches that more than one structure is formed in the substrate [col. 4, lines 38-42].

However, Chang et al. fails to teach the limitation in which the doping process is split into two doping steps, one for forming the first region and the other for forming the

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second regions. It is noted that the transposition of process steps or the splitting of one step into two, where the processes are substantially identical or equivalent in terms of function, manner and result, was held to be not patentably distinguish the processes. Ex parte Rubin 128 USPQ 440 (Bd.App.1959). See also In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1946); and Altiris Inc. v. Symantec Corp., 65 USPQ2d 1865 (CAFC 2003). Thus, Chang et al. makes obvious the claimed steps since the doping process taught by Chang results in the formation of regions which are substantially identical or equivalent to the regions formed by process steps claimed by applicant.

Regarding claim 2, Chang et al. teaches an ONO structure (110,112,114) as the gate insulator [see fig. 6].

Regarding claims 3, 5, 12 and 15, Chang et al. teaches that the ONO structure is formed by growing silicon dioxide (110) from silicon comprising the edge surfaces and second regions of the substrate (108) [see col. 3, lines 59-63]; forming a silicon nitride layer (112) adjacent the edge surfaces [see col. 3, lines 64-66]; and forming silicon dioxide (114) on the silicon nitride [see col. 4, lines 6-10]; wherein the silicon nitride layer is a trapping layer [col. 3, lines 54-56].

Regarding claims 4 and 17. Chang et al. teaches forming polysilicon gate as the control gate (116) [see col. 4, lines 24-25].

Regarding claims 6 and 14, Chang et al. teaches that the respective structures each configured to store more than one bit per memory cell [It is noted that the structure disclosed by Chang et al is identical to the structure claimed by applicant, hence it is inherent that the structure of Chang et al. stores more than one bit per memory cell, as required by applicant.]

Regarding claim 9, Chang et al. teaches that the semiconductor substrate comprises silicon [Chang teaches that Silicon dioxide layer (110) is formed by thermal oxidizing the substrate (col. 3, lines 56-63). Thus, it is obvious that the substrate (100) comprises silicon].

Regarding claim 19, Chang et al. teaches a NROM structure which inherently provides an electronic memory function by storing holes [see col. 1, lines 40-46].

Response to Arguments

7. Applicant's arguments with respect to claims 1-6, 9, 11-12, 14-15, 17, 19-22 have been considered but are most in view of the new ground of rejection.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KENNETH PARKER
SUPERVISORY PATENT EXAMINER

José R. Díaz Examiner Art Unit 2815